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09/931,887	08/20/2001	Shinji Shiraga	35.C15684	4036

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EXAMINER	
SURYAWANSHI, SURESH	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/931,887	SHIRAGA ET AL.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/15/05 amendments*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-49* is/are rejected.

7)☒ Claim(s) *44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 are cancelled.

2. New claims 28-49 are presented for examination.

Claim Objections

3. Claim 44 is objected to because of the following informalities: it is labeled as "Currently Amended", but it is a newly added claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 28-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thoulon (US Patent No. 6,128,747) in view of Applicant Disclosed Background of the Invention (ADBI).

6. As per claim 28, Thoulon discloses an information apparatus comprising:

processing means [Fig. 1; processor]; and

mode setting means for setting a mode of a memory [Fig. 1; col. 2, lines 18-24; col. 3, line 65 -- col. 4, line 8; means for setting the memory into its low power mode, i.e., the memory controller],

wherein said mode setting means sets the memory in a power mode in accordance with a signal which relates to the setting of said processing means in the power saving mode and inputted to said mode setting means while said mode setting means is in the enabled state [Fig. 1; col. 2, lines 18-24; col. 3, line 65 -- col. 4, line 8; the memory controller sets the memory into a power saving mode according to the acknowledgement signal that relates to the setting of the processing means in the power saving mode].

Thoulon does not expressly disclose that the processing means commands the memory to issue a power saving mode transfer instruction for setting the processing means in a power saving mode. However, ADBI clearly indicates that in order for the processing means to transfer to the power saving mode, it is necessary to execute a WAITI command. This WAITI command is stored in the main memory [page 1, line 27 -- page 2, line 18]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the processing means commands the memory to issue the power saving mode transfer instruction for setting the processing means in the power saving mode because commands are stored in the memory.

7. As per claim 33, Thoulon discloses an information processing apparatus comprising:

processing means [Fig. 1; processor]; and

mode transfer means for transferring a mode of a memory [Fig. 1; col. 2, lines 18-24; col. 3, line 65 -- col. 4, line 8; means for setting the memory into its low power mode, i.e., the memory controller],

wherein said mode transfer means transfers the memory to a power saving mode [Fig. 1; col. 2, lines 18-24; col. 3, line 65 -- col. 4, line 8; the memory controller sets the memory into a power saving mode according to the acknowledgement signal that relates to the setting of the processing means in the power saving mode].

Thoulon does not expressly disclose that the processing means sets the mode transfer means in a waiting state. However, ADBI clearly indicates that the processing means executes a WAITI command. This WAITI command is stored in the main memory so that the main memory is required to be in the normal operation mode when the WAITI command is fetched [page 1, line 27 -- page 2, line 18]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the processing means sets the mode transfer means (i.e., the memory controller) in a waiting state because the WAITI command is stored in the main memory.

8. As per claim 39, Thoulon discloses a power saving controlling method for a processor and a memory, the method comprising:

an enable state setting step of setting a memory controller for controlling the memory in an enable state [Fig. 1; col. 2, lines 18-24; col. 3, line 65 -- col. 4, line 8; acknowledgement signal detection step by the memory controller] ;

a power saving mode setting step of setting the memory in a power saving mode in accordance with a signal which relates to the setting of the processor in the power saving mode and inputted to the memory controller while memory controller is in the enable state [Fig. 1; col. 2, lines 18-24; col. 3, line 65 -- col. 4, line 8; the memory controller sets the memory into a power saving mode according to the acknowledgement signal that relates to the setting of the processing means in the power saving mode].

Thoulon does not expressly disclose that a requesting step of commanding the memory to issue therefrom a power saving mode transfer instruction for setting the processor in a power saving mode. However, ADBI clearly indicates that in order for the processing means to transfer to the power saving mode, it is necessary to execute a WAITI command. This WAITI command is stored in the main memory [page 1, line 27 -- page 2, line 18]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the processing means commands the memory to issue the power saving mode transfer instruction for setting the processing means in the power saving mode because the instruction is stored in the memory.

9. As per claim 44, Thoulon discloses a power saving controlling method for a processor and a memory, the method comprising:

a setting step of setting a memory controller for controlling the memory [Fig. 1; col. 2, lines 18-24; col. 3, line 65 -- col. 4, line 8; acknowledgement signal detection step by the memory controller];

a transferring step of transferring the memory to a power saving mode [Fig. 1; col. 2, lines 18-24; col. 3, line 65 -- col. 4, line 8; the memory controller sets the memory into a power saving mode according to the acknowledgement signal that relates to the setting of the processing means in the power saving mode].

Thoulon does not expressly disclose about a waiting state. However, ADBI clearly indicates that the processing means executes a WAITI command. This WAITI command is stored in the main memory so that the main memory is required to be in the normal operation mode when the WAITI command is fetched [page 1, line 27 -- page 2, line 18]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the processing means sets the mode transfer means (i.e., the memory controller) in a waiting state because the WAITI command is stored in the main memory.

10. As per claim 29, Thoulon discloses detecting means for detecting an instruction fetch transfer for the power saving mode transfer instruction and outputting the signal in accordance with detection of the instruction fetch transfer for the power saving mode transfer instruction, and wherein said mode setting means sets the memory in the power saving mode in accordance with the signal inputted from said detecting means while said mode setting means is in the enabled state [Fig. 1; col. 2, lines 18-24; col. 3, line 65 -- col. 4, line 8; the memory controller sets the memory into a power saving mode according to the acknowledgement signal that relates to the setting of the processing means in the power saving mode].

11. As per claim 30, Thoulon discloses if said processing means detects an interruption for returning to the normal operation mode from the power saving mode, said processing means returns a normal operation mode from the power saving mode and invalidates the signal relating to the setting of said processing means in the power saving mode [col. 2, lines 56-57; col. 4, lines 51-58; de-assertion of the sleep signal], and

wherein said mode setting means sets the memory in a normal operation mode in accordance with invalidation of the signal relating to the setting of said processing means in the power saving mode [col. 2, lines 56-61; col. 4, lines 51-58; waking up the memory].

12. As per claim 31, Thoulon discloses that said processing means outputs the signal for notifying said mode setting means that said processing means is transferred to the power saving mode [col. 2, lines 18-24, 52-55; acknowledgement signal], and

wherein said mode setting means sets the memory in the power saving mode in accordance with the signal inputted from said processing means while said mode setting means is in the enabled state [Fig. 1; col. 2, lines 18-24; col. 3, line 65 -- col. 4, line 8; the memory controller sets the memory into a power saving mode according to the acknowledgement signal that relates to the setting of the processing means in the power saving mode].

13. As per claims 32, 38 and 49, Thoulon discloses the invention substantially. Thoulon does not expressly disclose that the memory is set in the power saving mode after an end of memory transfer in progress. However, ADBI clearly indicates that the processing means executes a WAITI command. This WAITI command is stored in the main memory so that the main memory is required to be in the normal operation mode when the WAITI command is fetched [page 1, line 27 -- page 2, line 18]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the processing means sets the mode transfer means (i.e., the memory controller) in a waiting state because the WAITI command is stored in the main memory.

14. As per claim 34, Thoulon discloses that said mode transfer means supplies the memory with a predetermined signal to transfer to the memory to the power saving mode from a normal operation mode [Fig. 1; col. 2, lines 18-24; col. 3, line 65 -- col. 4, line 8; the memory controller sets the memory into a power saving mode according to the acknowledgement signal that relates to the setting of the processing means in the power saving mode].

15. As per claim 35, Thoulon discloses that said mode transfer means transfers the memory to a normal operation mode in accordance with an interruption for returning said processing means to a normal operation mode from the power saving mode [col. 2, lines 56-61; col. 4, lines 51-58; waking up the memory].

16. As per claims 36 and 47, Thoulon discloses the invention substantially. Thoulon does not expressly disclose about a waiting state. However, ADBI clearly indicates that the processing means executes a WAITI command. This WAITI command is stored in the main memory so that the main memory is required to be in the normal operation mode when the WAITI command is fetched [page 1, line 27 -- page 2, line 18]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the processing means sets the mode transfer means (i.e., the memory controller) in a waiting state because the WAITI command is stored in the main memory.

17. As per claims 37 and 48, Thoulon discloses the invention substantially. Thoulon does not expressly disclose about a waiting state. However, ADBI clearly indicates that the processing means executes a WAITI command. This WAITI command is stored in the main memory so that the main memory is required to be in the normal operation mode when the WAITI command is fetched [page 1, line 27 -- page 2, line 18]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the processing means sets the mode transfer means (i.e., the memory controller) in a waiting state because the WAITI command is stored in the main memory.

18. As per claim 40, Thoulon discloses a power saving controlling method according to claim 39, further comprising:

a detecting step of detecting an instruction fetch transfer for the power saving mode transfer instruction [col. 2, lines 18-24, 52-58]; and

an outputting step of outputting the signal in accordance with detection of the instruction fetch transfer for the power saving transfer instruction [col. 2, lines 18-24, 52-58],

wherein the memory is set in the power saving mode at said enable state setting step in accordance with the signal outputted in said detecting step while the memory controller is in the enable state [col. 2, lines 18-58; col. 3, lines 4-12].

19. As per claim 41, Thoulon discloses a power saving controlling method according to claim 39, further comprising:

a returning step of returning the processor to a normal operation mode from the power saving mode in accordance with an instruction [col. 2, lines 56-57; col. 4, lines 51-58; de-assertion of the sleep signal];

an invalidating step of invalidating the signal relating to the setting of the processor in the power saving mode in accordance with the returning to the normal operation mode of the processor [col. 2, lines 56-57; col. 4, lines 51-58; de-assertion of the sleep signal]; and

a returning step of returning the memory to a normal operation mode in accordance with invalidation of the signal relating to the setting of the processor in the power saving mode [col. 2, lines 56-61; col. 4, lines 51-58; waking up the memory].

20. As per claim 42, Thoulon discloses a power saving controlling method according to claim 39, further comprising an outputting step of outputting the signal for notifying memory controller that the processor is transferred to the power saving mode [col. 2, lines 18-24, 52-55; acknowledgement signal], and

wherein the memory is set in the power saving mode at said power saving mode setting step in accordance with the signal outputted at said outputting step while said mode setting means is in the enabled state [Fig. 1; col. 2, lines 18-24; col. 3, line 65 -- col. 4, line 8; the memory controller sets the memory into a power saving mode according to the acknowledgement signal that relates to the setting of the processing means in the power saving mode].

21. As per claim 43, Thoulon discloses the invention substantially. Thoulon does not expressly disclose that the memory is set in the power saving mode after an end of memory transfer in progress. However, ADBI clearly indicates that the processing means executes a WAITI command. This WAITI command is stored in the main memory so that the main memory is required to be in the normal operation mode when the WAITI command is fetched [page 1, line 27 -- page 2, line 18]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the processing means sets the mode transfer means (i.e., the memory controller) in a waiting state because the WAITI command is stored in the main memory.

22. As per claim 45, Thoulon discloses that said transferring step supplies the memory with a predetermined signal to transfer the memory to the power saving mode from a normal operation mode [Fig. 1; col. 2, lines 18-24; col. 3, line 65 -- col. 4, line 8; the memory controller sets the memory into a power saving mode according to the acknowledgement signal that relates to the setting of the processing means in the power saving mode].

23. As per claim 46, Thoulon discloses a returning step of returning the memory to a normal operation mode in accordance with an interruption for returning the processor to a normal operation mode from the power saving mode [col. 2, lines 56-61; col. 4, lines 51-58; waking up the memory].

Response to Arguments

24. Applicant's arguments with respect to claims 28-49 have been considered but are moot in view of the new ground(s) of rejection. Theses are new claims, which are presented first time.

Conclusion

25. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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September 26, 2005